REMARKS

Claims 1, 2, 4-9, 11-15, and 17-20 are presently pending. Claims 3, 10, and 16 are cancelled without prejudice. Claim 21 is added. Assignee respectfully requests reconsideration.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being obvious from Holcombe (U.S. Pat. Pub. No. 2005/0105883), and Kato. Claim 1 recites, among other limitations, "wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input".

The Office Action indicates that "Holcomb teaches … wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced. [fig. 6 P 0095 P 0049] and logic for determining whether parameters receved by the input are valid, wherein the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced. [Fig. 6; P 0095]."

Holcomb teaches that "The conditions for valid *entry points* differ depending on how the picture has been encoded (progressive, field interlaced, or frame interlaced)." Entry points are further discussed in paragraph 0035. However, it is clear that in Holcomb, whether the picture is a valid entry point or not does not determine whether the parameters are valid or not. In fact, from paragraph 0035, a picture that is not a valid entry point can be a valid picture with valid parameters. Accordingly, for the foregoing reason alone, Appellant traverses the rejections to claims 1, 8, and 13.

Additionally, even if Holcomb were modified to included counting the number of motion vectors, neither Holcomb or Kato provide any criteria, rules, or algorithms that explain to one of ordinary skill in the art, how "the logic determines whether the parameters received by the input are valid based on the picture type indicator, whether the picture is progressive or interlaced, and the number of motion vectors received by the input". How would "The conditions for valid entry points" be modified to take into the number of vector(s)? Neither reference addresses this.

For this additional reason, Assignee also traverses the rejection to claim 1, 8, and 13.

Claim 5 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Holcomb and Kato in view of Kim. Claim 5 recites, among other limitations, "wherein the control register comprises one or more bits, each of which are associated with a corresponding

one or the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

The Office Action indicates that Kim teaches the foregoing, at [col. 5, line 57-col. 6, lines 20; Abstract; Col. 1 lines 44-57; Fig. 1; Fig. 4; Fig. 6; Col. 6 Lines 8-12; col. 5 lines 57-col. 6 lines 20].

Although in Kim, Abstract, the "motion vector decoder" includes a number of things, e.g., "a parameter delay block", "a motion vector residual block", "motion vector code table", etc., Kim abstract does not teach anything that "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Moreover, Kim, Col. 6, Lines 8-12 recites that:

> The vlc[10:0], shown in FIG. 2(e), is a MV value variable length coded by the encoder and is received by the MV residual block 11 and the MV code table block. Since maximum of 11 data bits may be produced through the VLC, the vlc[10:0] has a length of 11 bits and is the most significant bit (msb). The msb value may or may not be sent by the encoder and if sent, one or all eight values may be sent.

(Emphasis Added). It is noted that Kim does not tech that "vlc[10:0]" "comprises one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers". Moreover, it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be obtained per macroblock" at Col. 1, Line 44. Thus vlc[10:0] does not "comprise[s] one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector".

Examiner has also indicated that "Kim discloses 8 bit number in the residual value. [col. 5 line 57 –col. 6 line 20]". Office Action at 2. Assignee has not disputed that Kim discloses "one or more bits", rather, Assignee traverses the finding that Kim discloses one or more bits, each of which are associated with a corresponding one of the one or more motion vector registers, wherein the one or more bits are in a particular state, based on whether the corresponding motion vector register stores a motion vector". The argument in the above paragraph (it is noted that "vlc" appears to have 11 bits, "[10:0]", while also indicating that "A maximum of 4 MVs can be

obtained per macroblock" at Col. 1, Line 44…) would apply the same to 8 bits.

Accordingly, Appellant requests traverses the rejection to claim 5. Additionally, Assignee requests allowance of claim 21.

CONCLUSION

For at least the foregoing reasons, Assignee respectfully submits that each of the pending claims are allowable and Examiner is respectfully requested to pass this case to issuance. The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,

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